Analysis and Characterization of Variability in Subthreshold Source-Coupled Logic Circuits

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***Abstract*—This article explores the effect of device parameter variations on the performance of subthreshold source-coupled logic (STSCL) circuits. A test chip has been fabricated in a standard CMOS 90 nm technology to study the matching properties of STSCL circuits. Both process variations and device mismatch have been included in this study. The performed analysis shows that while the STSCL topology is very robust against global variations mainly thanks to the adoption of an on-chip bias generator circuit, special design techniques are required to compensate for the effect of device mismatch. Proper device sizing as well as creating intentional mismatch in the biasing condition of STSCL gates are two effective approaches that have been investigated to overcome the variation related issues. Both die-to-die (D2D) and within-die (WID) variations in the delay of STSCL gates have been characterized and validated through measurements. A comprehensive analysis of timing jitter in STSCL-based ring oscillators is also presented.**

***Index Terms*—Jitter, mismatch, ring oscillator, source-coupled logic (SCL), subthreshold SCL (STSCL), ultra-low power (ULP) circuits, variability.**

I. Introduction

PROCESS variations and leakage are two major limits to reduce the energy consumption in a given technology node [1]–[5]. Many different techniques have been studied and proposed in order to reduce or control these two effects. Device up-sizing and increasing the supply voltage are two well-known approaches for reducing the effect of variability [6]–[8]. Meanwhile, using multi-threshold voltage MOS devices, body biasing, and many other techniques have been proposed to control the leakage power dissipation [9]–[11].

Recently, the subthreshold source-coupled logic (STSCL) topology has been introduced as an alternative circuit approach for implementing ULP digital systems [see Fig. 1(a)] [7], [12], [13]. In this type of logic circuits, the input differential pair is biased in subthreshold regime. Having a good control of the current consumption of each logic cell enables reducing the power dissipation of each gate down to few picowatts, i.e., significantly below the leakage current level in static CMOS circuits in modern UDSM technologies [7]. Fig. 1(b) and (c) illustrate the design space of the STSCL topology in comparison to the static CMOS logic. In CMOS logic, there is a tight tradeoff among circuit parameters, performance parameters, and process parameters which can heavily constrain the design optimization [14]. On the other hand, the design of STSCL gates is more relaxed mainly thanks to the independence of delay to supply voltage and to device parameters such as threshold voltage (V_{TH}) and gate oxide thickness (t_{ox}). Thereby, it is possible to choose the optimal device and circuit parameters targeting a minimum energy consumption level without affecting the gate delay. This flexibility makes system level design and power management easier to handle and more effective, when aggressive requirements on the consumption are targeted.

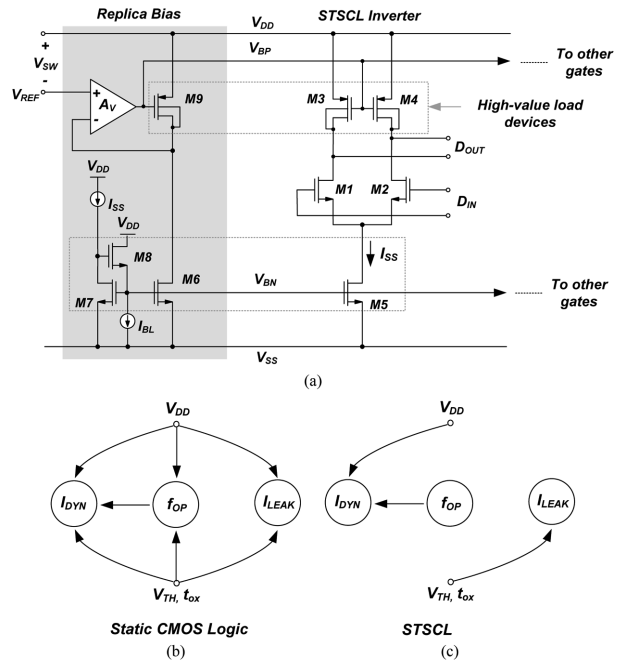

Fig. 1. (a) A subthreshold SCL gate and its replica bias circuit used to control the output voltage swing [7]. Design space of: (b) static CMOS, and (c) STSCL styles.

In this paper, the sensitivity of the STSCL topology to device parameter variation and mismatch is analyzed and studied. As further shown, this topology shows little dependence on global process variations, supply voltage, and temperature (PVT) variations. This property mainly originates from the use of an on-chip bias current generator circuit, which compensates the effect of global PVT variations. However, device parameter mismatches can affect the performance of STSCL circuits.

Manuscript received June 18, 2014; revised September 01, 2014; accepted September 30, 2014. Date of publication November 12, 2014; date of current version January 26, 2015. This work was supported in part by the Swiss Nano-Tera Program NTF project: ULP-Systems. This paper was recommended by Associate Editor V. Chandra.

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Digital Object Identifier 10.1109/TCSI.2014.2364101

Therefore, a variation-aware device sizing is required to guarantee proper circuit operation and performance in large-scale and mass produced implementations with adequate parametric yield. This paper also proposes some techniques for reducing the sensitivity of STSCL circuits to device mismatch.

This paper is organized as follows. Section II provides an overview on STSCL circuits. The effect of random variations on the STSCL topology is studied in Section III. Solutions to mitigate the impact of variations on STSCL circuits are discussed in Section IV. Section V analyzes the behavior of STSCL circuits in the presence of global PVT variations. The test chip description is presented in Section VI. The experimental results to validate the theoretical findings and provide full characterization of variations are presented in Section VII, and Section VIII concludes the paper.

II. STSCL Circuits

The schematic of an STSCL inverter is shown in Fig. 1(a). The operation of STSCL circuits is similar to the conventional SCL (or current-mode logic, CML) circuits [15]–[17]. In this topology, the logic operation takes place in current domain based on the polarity of the input signal, D_{IN}. Then the output current is converted back to voltage domain (D_{OUT}) by the load resistances. Very high-value load devices are required since current levels are extremely low (as low as a few picoamperes) in STSCL topology. As depicted in Fig. 1(a), these load resistors can be implemented using drain to bulk shorted PMOS devices [7]. A simplified circuit diagram of the replica bias (RB) circuit used to control the output voltage swing is also shown [7]. The replica bias circuit generates the bias voltage for the NMOS tail transistor and the PMOS load devices [12].

The transconductance of a differential pair circuit operating in subthreshold regime can be estimated by [7], [18]:

$$G_m = \frac{\partial I_{OUT}}{\partial D_{IN}} = \left(\frac{I_{SS}}{2n_n U_T}\right) \cdot \frac{1}{\cosh^2\left(\frac{D_{IN}}{(2n_n U_T)}\right)} \quad (1)$$

where D_{IN} indicates the input differential voltage, n_n is the subthreshold slope of the NMOS devices, and U_T stands for the thermal voltage. Based on (1), for $D_{IN} > 4n_n U_T$ the entire tail current will be switched to one of the output branches. Therefore, a voltage swing of more than $4n_n U_T$ is needed to guarantee that the gain of the STSCL circuit is sufficiently large to be used as a logic gate. The value of the load resistance can be estimated by:

$$R_{SD} = \frac{n_p U_T}{I_{SD}} \cdot \frac{e^{\frac{V_{SD}}{U_T}} - 1}{(n_p - 1)e^{\frac{V_{SD}}{U_T}} + 1} \quad (2)$$

where n_p is the subthreshold slope of PMOS devices [7]. Combining (2) with (1) results in [7]:

$$A_V = G_m \cdot R_{SD} \leq \frac{n_p}{n_n \cdot (n_p - 1)}. \quad (3)$$

These equations are essential in studying the effect of variations in the STSCL topology, which is presented in the following Sections.

III. Impact of Random Variations on STSCL Circuits

Parameter variations can affect the circuit performance parameters such as delay (speed) and power dissipation, as well as the circuit robustness. Operating in subthreshold regime, the effect of variability can be even more pronounced, due to the exponential I/V characteristics of the MOS devices. In the following, the effect of variability on robustness and delay of STSCL circuits is studied.

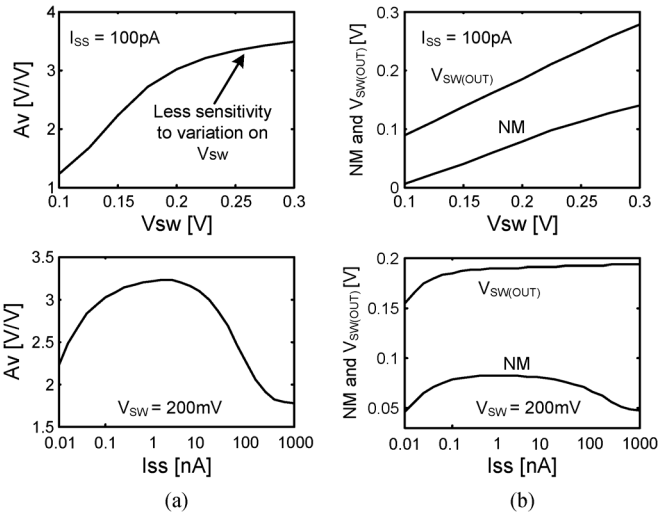

Fig. 2. DC transfer characteristics of an STSCL circuit. (a) Differential DC gain versus desired V_{SW} and tail bias current. (b) Noise margin and output voltage swing versus V_{SW} and tail bias current.

A. Noise Margin of STSCL Circuits

Generally, the robustness of a logic gate against external or internal perturbations is indicated by the noise margin (NM) [19], [20]. NM is measured in quasi-static operating conditions and represents the maximum perturbation amplitude in voltage units that does not influence the logic state of the circuit.

In a subthreshold SCL circuit with ideal load resistors, it can be shown that the NM is [12]:

$$\frac{NM}{V_{SW}} = \sqrt{1 - \frac{1}{A_V}} - \frac{1}{A_V} \cdot \tanh^{-1}\left(\sqrt{1 - \frac{1}{A_V}}\right). \quad (4)$$

where A_V represents the DC voltage gain of the circuit and V_{SW} is the single-ended voltage swing at the output. For typical values of DC voltage gain of an STSCL circuit (in the range of 2.8 to 3.3), NM can be as high as approximately 40% of the entire output voltage swing.

The output voltage swing, peak gain value, and noise margin of an STSCL buffer versus V_{SW} and tail bias current (I_{SS}) are shown in Fig. 2. As illustrated in these figures, gain and NM are both improving by increasing V_{SW}. For voltage swing values higher than 200 mV, the gain improvement tapers off. This phenomenon can also be interpreted as a reduced sensitivity of the voltage gain to the voltage swing. Otherwise stated, STSCL gates with a voltage swing larger than 200 mV show a robust DC characteristics. This property is further exploited to reduce the circuit sensitivity to the device mismatch effects. Replacing $(A_V \approx 3.2)$ in (4) results in $NM \approx 0.5 \cdot V_{SW}$, which is in close agreement with the graph plotted in Fig. 2(b).

Referring to Fig. 1(a), it is clear that the output voltage swing should always be smaller than the gate-source voltage (V_{GS}) of the NMOS differential pair devices. Otherwise, current switching in the differential pair circuit will not be complete.

Based on Fig. 2, in high current density conditions, the devices enter into medium and strong inversion regions. Hence, the gain of the circuit degrades as well. For very low bias current values, the tail bias current becomes comparable to the level of

the leakage current sources in the circuit which results in performance degradation. It is noticeable that $NM \gg 0$ for tail bias current values of as low as 10 pA, meaning that the bias current can be reduced to this level without jeopardizing the signal integrity.

B. Impact of Variations on Noise Margin

Noise margin degrades due to device mismatch and process variations.[1] Variation of the output voltage swing as well as voltage offset at the input of STSCL circuits are the two main causes of NM reduction in the presence of device mismatch. In practice and in the presence of device mismatch, the noise margin can be estimated by:

$$NM \approx NM_{nominal} - \left(\frac{\partial NM}{\partial V_{SW}}\right) \cdot \Delta V_{SW} - V_{OS}. \quad (5)$$

where $NM_{nominal}$ is the NM without device mismatch, and V_{OS} is the equivalent input-referred offset of the STSCL gate. The noise margin is degraded by the variations in the load transistors M_3 and M_4 in Fig. 1(a), as well as the mismatch in the source-coupled pair. Assuming moderate variations in the resistance of M_3 and M_4 (and hence V_{SW}), and considering that the offset voltage of M_1 and M_2 directly subtracts from the available noise, the noise margin in the presence of variations can be expressed as:

$$\frac{\partial NM}{\partial V_{SW}} = \sqrt{1 - \frac{1}{A_V}}. \quad (6)$$

From (5), for uncorrelated random variations on the offset voltage and voltage swing (i.e., between $M_{1,2}$ and $M_{3,4}$), the degradation of NM can be expressed by:

$$\Delta NM^2 \approx \left(\frac{\partial NM}{\partial V_{SW}} \Delta V_{SW}\right)^2 + V_{OS}^2. \quad (7)$$

On the other hand, the input-referred offset of the source-coupled pair M_1 and M_2 in Fig. 1(a) is:

$$\sigma_{OS}^2 \approx \left(\frac{A_{VT,N}^2}{W_N L_N}\right) + \left(\frac{A_{VT,P}^2}{W_P L_P}\right) \times \left(\frac{n_n}{n_p}\right)^2 \quad (8)$$

where A_{VT} represents the threshold voltage variation per unit micrometer square area of the gate terminal, W and L are the width and length of M_1 and M_2, respectively.

The variation of V_{SW} that is affecting the noise margin based on (7), can be caused by the tail bias current mismatch and the mismatch between PMOS load devices of the STSCL circuits and the replica bias circuit:

$$\sigma_{SW}^2 \approx \left(\frac{n_p}{n_p - 1}\right)^2 \cdot \left(\frac{A_{VT,N}^2}{n_n^2 W_B L_B} + \frac{A_{VT,P}^2}{n_p^2 W_P L_P}\right) \quad (9)$$

where W_B, L_B are the width and length of the tail bias transistors, and W_p, L_p are the width and the length of the PMOS load devices.

Monte Carlo simulation results of an STSCL gate are shown in Fig. 3. This figure shows the variation of the maximum DC gain, noise margin, output voltage swing, and the input-referred offset of the STSCL circuit. There is a good agreement between the Monte Carlo simulation results depicted in Fig. 3 and hand calculations based on (8), both resulting in $3\sigma \approx 20$ mV for the input-referred offset. In addition, the scattering plots in Fig. 4 depict: (a) the correlation between the variation of noise margin and offset voltage, and (b) the correlation between noise margin and output swing variation.

[1]In this paper, device mismatch and process variations refer to the random within-die and die-to-die variations, respectively.

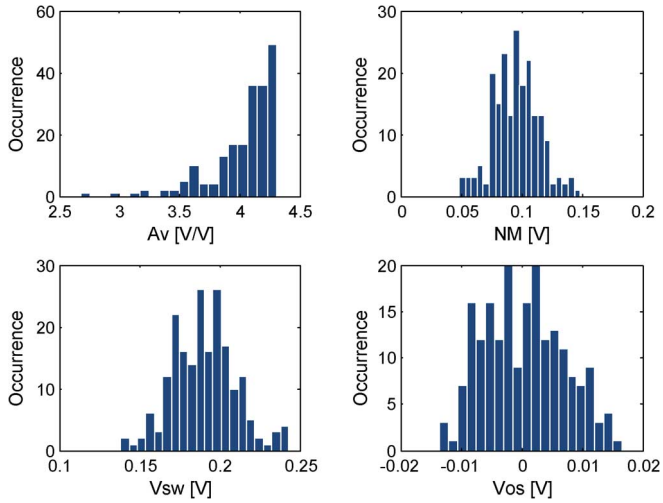

Fig. 3. Mismatch effect on STSCL gate performance. Variation on gain, NM, voltage swing, and input-referred offset are shown. The value of NM highly depends on the output voltage swing. Here, $V_{SW} = 200$ mV and $I_{SS} = 100$ pA, for 200 runs of Monte Carlo simulations.

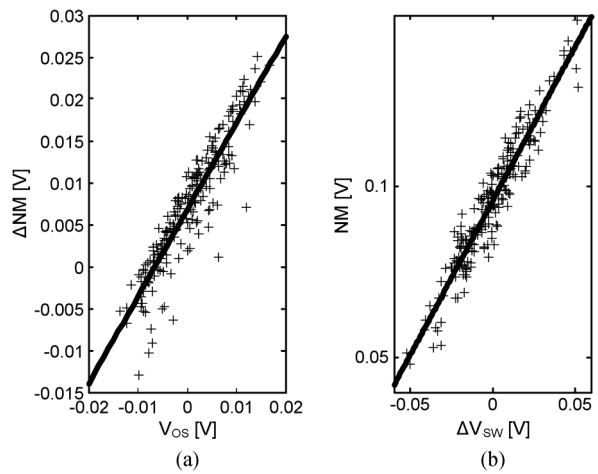

Fig. 4. Correlation between: (a) variation on NM and offset voltage, (b) NM and output swing variation, based on Monte Carlo simulations.

Assuming that $A_{VT,P} \approx A_{VT,N} \approx A_{VT}$ and $n_p \approx n_n$, then:

$$\left(\frac{\sigma_{NM}}{A_{VT}}\right)^2 \approx \frac{1}{W_N L_N} + \frac{A_V(A_V - 1)}{W_B L_B} + \frac{A_V(A_V - 1) + 1}{W_P L_P} \quad (10)$$

C. Impact of Variations on Delay

Gate delay can vary from gate to gate due to the device mismatch effects. Mismatch of the tail bias current and the load resistances are the main sources of delay variation in the STSCL topology. Assuming that the load resistance can be approximated by:

$$R_L \approx \frac{V_{SW}}{I_{SS}} \quad (11)$$

the variation of the STSCL gate delay can be expressed by:

$$\frac{\Delta t_d}{t_d} \approx \frac{\Delta V_{SW}}{V_{SW}} - \frac{\Delta I_{SS}}{I_{SS}}. \quad (12)$$

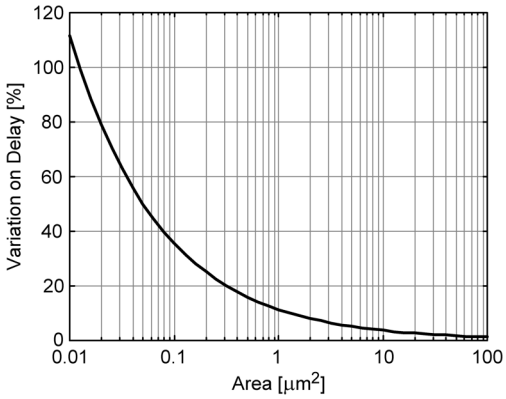

Fig. 5. Delay variation (within one standard deviation) due to the device mismatch based on (16). It is assumed that $A_{VT} = 5\ [\mathrm{mV} \cdot \mu\mathrm{m}]$, and the gate area of the PMOS load and tail bias NMOS devices are both equal to WL.

where the variation of the load capacitance has been ignored [18]. Rewriting the variation of the voltage swing as:

$$\Delta V_{SW} \approx \frac{\Delta V_{T,P}}{n_p - 1} + \frac{n_p U_T}{n_p - 1} \times \frac{\Delta I_{SS}}{I_{SS}} \tag{13}$$

then, the variation of delay is:

$$\left(\frac{\Delta t_d}{t_d}\right)^2 \approx \left(\frac{\Delta I_{SS}}{I_{SS}}\right)^2 \times \left(\frac{n_p}{n_p - 1} \cdot \frac{U_T}{V_{SW}} - 1\right)^2 \left(\frac{\Delta V_{T,P}}{V_{SW}} \cdot \frac{1}{n_p - 1}\right)^2 \tag{14}$$

where the variation on tail bias current is [21]:

$$\frac{\Delta I_{SS}}{I_{SS}} \approx \frac{\Delta V_{T,N}}{n_n U_T} \tag{15}$$

Based on (13), any mismatch of the tail bias current affects the voltage swing variation at the output. By reducing (increasing) the tail bias current, the output voltage swing will also reduce (increase) and based on the first term in (12), the gate delay will decrease (increase) accordingly. However, at the same time, the available current for discharging the output parasitic capacitance will be reduced (increased) which results in a delay increase (reduction), based on the second term of (12). Therefore, the variation of the tail bias current imposes two opposite effects on delay which partially cancel out each other [see (14)].

To have a very approximate estimation of the delay variation due to the device mismatch in the STSCL topology, and assuming that $A_{VT,N} = A_{VT,P}$ and the area of the PMOS load device $(W_p L_p)$ and tail bias device $(W_B L_B)$ are equal $(W_p L_p = W_B L_B = WL)$, yields:

$$\frac{\Delta t_d}{t_d} \approx \frac{A_{VT}}{n_n U_T} \cdot \frac{1}{\sqrt{2WL}}. \tag{16}$$

The approximate variation of the gate delay for different gate area values is shown in Fig. 5.

IV. Techniques to Mitigate the Impact of Variations on STSCL Circuits

Approaches to reduce the sensitivity of the STSCL circuits to device mismatch are discussed in this section. Equation (10) expresses the tradeoff between area and robustness, and can also be used for variation-aware transistor sizing of STSCL cells. In particular, it is useful to observe that the area of an STSCL circuit depends on A_{VT}, for a given robustness target. In detail, from the perspective of technology scaling, it is expected that the size of STSCL cells can be scaled down in proportion to the improvement in A_{VT} value. As generally the improvement on A_{VT} is slower than the shrinking of the gate length, the size of STSCL gates cannot be scaled down as aggressively as the minimum feature size does.

In addition, (10) and (16) show the importance of well-matched bias current distribution between STSCL gates. Indeed, in these equations, the matching of the PMOS load devices and tail bias transistors are significantly more important than the device parameter matching of the NMOS differential pair. Also, according to (16), the delay variability for minimum-sized devices can be very high. Hence, non-minimum sized transistors need to be considered in practical cases, to keep robustness within reasonable bounds.

In the following, various approaches to mitigate the impact of transistor mismatch are discussed.

The first knob that can be leveraged to mitigate the impact of mismatch is V_{SW}. Indeed, as illustrated in Fig. 2, the variation of the DC gain of STSCL circuits decreases for $V_{SW} > 200\ \mathrm{mV}$. Therefore, based on (4), the circuit exhibits less variation of noise margin.

Another approach to reduce the sensitivity of NM to variations is to create intentional mismatch between the replica bias and the STSCL gates. If the bias current of each cell increases by approximately 20% compared to the replica bias circuit, for example, then the voltage swing in STSCL gates will increase by the same percentage compared to the V_{SW} in the RB circuit. Therefore, the initial NM will be larger and more robust against process variation. Although this approach increases the circuit power dissipation by about 20%, this effect can be partially compensated by using smaller devices. The analysis shows that using slightly higher current in STSCL gates compared to the replica bias circuit considerably reduces the variation on the gain of the cells with respect to the process variations (i.e., $\partial A_V / \partial V_T$), which in turn increases the resistance of NM against process variations. This effect is evident from Fig. 2(a). In this figure, values of the voltage swing larger than 200 mV lead to a considerable reduction in the variation of the voltage gain. Therefore, less variation on the noise margin is expected. As shown in Fig. 2(a), the variation of A_V versus V_{SW} is approximately four times smaller for $V_{SW} > 200\ \mathrm{mV}$, compared to the case where $V_{SW} < 200\ \mathrm{mV}$.

A controlling circuit is necessary to keep the voltage swing at the output of STSCL gates at a desired value. If V_{SW} decreases, NM will degrade and if V_{SW} increases, the gate delay will proportionally increase. Hence, V_{SW} should be selected close to its optimum value. A replica bias circuit is employed as an efficient approach to suppress the impact of variations on STSCL circuits.

The schematic of the replica bias circuit has been shown in Fig. 1(a). The replica bias circuit needs to be sufficiently precise. Thus, the amplifier A_V in Fig. 1(a) should provide enough gain with a very low offset to guarantee the desired accuracy. A folded-cascode amplifier has been used to provide a large output voltage swing and to enable operation of the SCL gates in a very wide range of bias current values. The STSCL gate used inside the replica bias circuit should be well matched to the STSCL gates being biased to have very low deviation from the desired operating point. Any mismatch between the bias current of the

devices in STSCL gates and the corresponding devices in RB circuit will result in variation of the desired output voltage swing (ΔV_{SW}).

Assuming that the load devices are biased in SI, then

$$I_{SD,M9} = \mu C_{ox}\frac{W}{L_e}\cdot V_{SD}\cdot\left(V_{SG} - |V_{T,P}| - \frac{V_{SD}}{2}\right)|_{V_{SD}=V_{SW}} \quad (17)$$

When the entire bias current flows through a PMOS load, the voltage drop across its source-drain is intended to be V_{SW}. Now, if there is any mismatch between the replica bias circuit and the SCL gate inside the circuit, the voltage swing at the output of this SCL gate will change as

$$\left(\frac{\Delta V_{SW}}{V_{SW}}\right)^2 = \left(\frac{1}{1+\frac{\beta\cdot V_{SW}^2}{2I_{SS}}}\right)^2 \times\left(\left(\frac{\Delta I_{SS}}{I_{SS}}\right)^2+\left(\frac{\Delta\beta}{\beta}\right)^2+\left(\frac{\beta V_{SW}\cdot\Delta V_{T,P}}{I_{SS}}\right)^2\right) \quad (18)$$

Regarding (18), to have an acceptable performance with required noise margin (NM), ΔV_{SW} should be kept as small as possible. This requires large enough NMOS tail bias transistors and PMOS load devices. Neglecting the mismatch due to β and adding amplifier offset, V_{OS}, the expression for ΔV_{SW} can be more simplified to

$$\left(\frac{\Delta V_{SW}}{V_{SW}}\right)^2 \approx \left(\frac{V_{OS}}{V_{SW}}\right)^2 + \left(\frac{1}{1+\frac{\beta V_{SW}^2}{2I_{SS}}}\right)^2 \times\left(\left(\frac{\Delta V_{T,P}}{V_{SG}-|V_{T,P}|-V_{SW}}\right)^2+\left(\frac{\Delta I_{SS}}{I_{SS}}\right)^2\right) \quad (19)$$

In general, a high enough value for V_{SW} should be selected in order to compensate the effect of variation at the output voltage swing and keep the NM on acceptable level.

Assuming $V_{SW} = R_L I_{SS}$, the sensitivity of this circuit to the mismatch is:

$$\left(\frac{\Delta V_{SW}}{U_T}\right)^2 \simeq \left(\frac{n_p}{n_p-1}\right)^2 \cdot\left(\left(\frac{\Delta I_{SD}}{I_{SD}}\right)^2+\left(\frac{\Delta\beta}{\beta}\right)^2+\left(\frac{\Delta V_{T0}}{n_p U_T}\right)^2\right) \quad (20)$$

in which $\beta = \mu C_{ox} W/L_e$. The amplifier offset should also be included in this estimation.

Monte Carlo simulations show that for minimum size devices, ΔV_{SW} can be as high as 20 to 40 mV in a typical 0.18 μm process. To compensate the influence of device mismatch, V_{SW} should be selected slightly larger than the minimum value. Meanwhile, it can be shown that the voltage gain from gate to drain of transistor M_9 in Fig. 1(a) is not very large:

$$|A_{V,M}| = g_{m,M9}\cdot R_{SD} \simeq \frac{1}{n_p-1}. \quad (21)$$

Therefore, in spite of the exponential relationship between $I_{SD,M9}$ and $V_{SG,M9}$, the gain of this stage is low and the RB circuit can be stabilized without difficulty.

One single replica bias circuit can be used for a large number (several hundreds) of STSCL gates, so that its area and consumption can be amortized over a large number of logic gates. Sharing a RB circuit among 10 000 cells leads to a typical area penalty of only 0.75%, compared to the case without RB circuit. Accordingly, the RB circuit permits to considerably improve the robustness against variations at rather small area penalty.

The level shifter constructed by M_8 and I_{BL} in Fig. 1(a), keeps the drain voltage of M_7 sufficiently large to operate at high enough V_{dsat} (overdrive voltage) levels and avoid entering into triode region, even at very low bias currents. The effect of the RB circuit and its relative positioning on the die with respect to the STSCL gates are studied in Section VII.

V. Effect of Global Variations on STSCL Circuits

The power dissipation of an STSCL-based system with an average logic depth of N is:

$$P_{diss,STSCL,N} \approx \ln 2 \times N^2 V_{DD} V_{SW} C_L f_{op} \quad (22)$$

where C_L stands for the average load capacitance at the output of STSCL gates and f_{op} indicates the system operation frequency [7], [13]. The delay of each STSCL gate can be approximated by:

$$t_d = \ln 2 \times R_L\cdot C_L \approx \ln 2 \times \left(\frac{V_{SW}}{I_{SS}}\right)\cdot C_L \quad (23)$$

where I_{SS} is the tail bias current of each cell. Considering (22) and (23), it can be concluded that the device parameters and especially threshold voltage do not influence the speed-power consumption tradeoff in SCL topology. The replica bias circuit will compensate for the effect of temperature and process variations [7]. Therefore, this topology exhibits a very low sensitivity to PVT or global variations.

The simulated gate delay versus load capacitance at different temperatures is shown in Fig. 6(a). The test chip was fabricated in 0.18 μm CMOS and included an STSCL based ring oscillator with a variable load capacitance. A binary weighted switched cap bank was used to set the value of the load capacitance and the oscillation frequency versus C_L was measured. Simulations show that the variation of gate delay due to the temperature variations is less than 5%. The results based on (23) and simulations agree very well with the measurements. The delay variation versus temperature over different process corners is shown in Fig. 6(b). Here, the delay values are normalized to the typical gate delay at 27 °C. Both graphs depict the low sensitivity of the STSCL topology to the global process and temperature variations.

VI. Test Chip Description

A second test chip has been fabricated in a standard CMOS 90 nm technology to study and measure the matching properties of STSCL circuits, by placing several ring oscillators with different distances to a common replica bias circuit (Fig. 7). As shown in [22], very well-matched delay elements are critical components for implementing high-precision ring-oscillator based quantizers. To achieve the desired dynamic range, the delay mismatch among delay stages in a ring oscillator needs to be sufficiently low. Based on (16), careful sizing of the load and bias tail devices is required to achieve the desired precision. As shown in Fig. 7, non-minimum load and tail transistors have been used to achieve the required accuracy.

The implemented test chip illustrated in Fig. 8 includes eight stand-alone ring oscillators to measure the on-die and die-to-die delay variations of the STSCL gates.

In this design, the tail bias current of each delay element can be tuned from 10 pA up to 10 nA using internal programmable

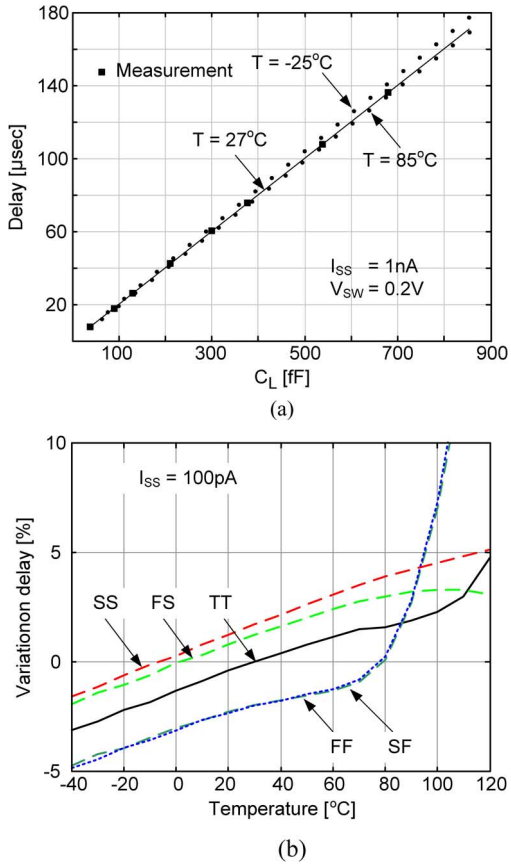

Fig. 6. (a) Dependence of gate delay on load capacitance at different temperatures, (b) delay variation vs. temperature over different corner cases.

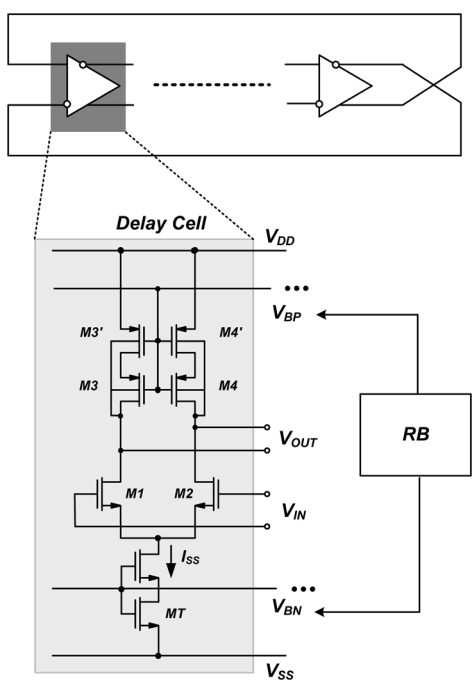

Fig. 7. Differential STSCL-based ring oscillator.

current mirrors. The oscillation frequency increases almost linearly with the controlling current. The voltage swing has been set to 200 mV, slightly larger than the theoretical limit $(4nU_T)$. Each ring oscillator approximately consumes 15 times the tail bias current, since the number of delay cells is $N_d = 15$. The

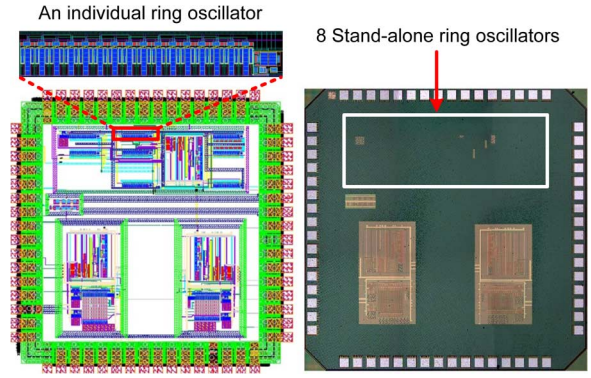

Fig. 8. Mask layout (left) and chip microphotograph (right) of the test chip in a CMOS 90 nm technology. This test chip includes two ring-oscillator based quantizers and eight stand-alone test ring oscillators.

size of the transistors has been selected sufficiently large, to guarantee less than 1% variation from the nominal oscillation frequency of the ring oscillators.

VII. Experimental Results and Characterization of Performance Variations

In this section, the measurement results for the test chip described in the previous section are reported. In particular, variations of the delay and the analysis of jitter are presented, based on the measurement of STSCL-based ring oscillators.

Device mismatch can be described by within-die and die-to-die variations. Unlike die-to-die (D2D) variations which affect all the transistors on a die almost equally, the within-die (WID) random and systematic variations can result in different effects on the transistors across a die [23], [24].

The placement of the ring oscillators on a sample die is shown in Fig. 9. This figure also illustrates the relative oscillation frequency of the ring oscillators based on the measurements on a single die. A clear gradient of the oscillation frequency is observed, which is mainly due to the gradient on the threshold voltage of the current mirrors. Not exactly similar profiles are observed in all nine measured dies, which indicates the random change of systematic WID variations from die to die. However, the shown profile is a fair representation of the oscillation frequency distribution on the majority of tested dies. Considering this effect, the position of the replica bias circuit seems to be important for the distribution of frequencies. This also reflects the importance of well-matched bias current distribution between STSCL gates. As shown in (10) and (16), the matching of the PMOS load devices and tail bias transistors are significantly more important than the device parameter matching of the NMOS differential pair. The maximum shift in measured oscillation frequency of the ring oscillators on a die is 1.4% with respect to the average frequency, which is much less than similar static CMOS inverter-based designs. This is a result of the relaxed matching properties of STSCL gates.

The overall variation (WID and D2D) of the oscillation frequency for more than 200 measurements at three different bias current levels are shown in Fig. 10. Each oscillation frequency has been normalized to the average oscillation frequency on each die, and the results of nine dies are used to plot these graphs. For different bias current levels, variations of the oscillation frequencies on one die and from die to die were observed. Higher frequency operation results in smaller deviation from

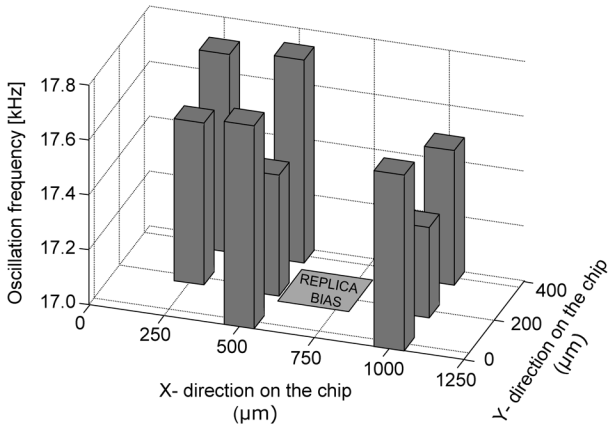

Fig. 9. Gradient effect on the frequency mismatch between oscillators on a die due to within-die variations. This figure also shows the relative placement of the ring oscillators on the die. The heights of columns are proportional to the oscillation frequency. The active area including the ring oscillators is 1250 μm $\times$ 400 μm.

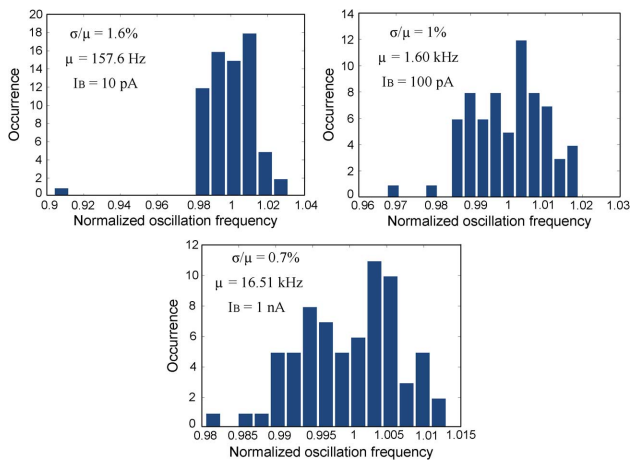

Fig. 10. Mismatch effect on oscillation frequency for 210 measurements on 9 dies with different bias current levels. Both D2D and WID variations are considered.

the mean value, while larger variations are observed at lower frequencies. The difference is due to the lower current levels resulting in inferior matching properties of the current mirrors biased in deep subthreshold region.

The standard deviation versus average oscillation frequency of different dies is shown in Fig. 11. D2D standard deviations at three bias conditions are also demonstrated in this figure. The sensitivity of frequency deviation to the current level is relatively constant for both types of variations. As shown in this figure, despite the relatively high D2D variations, the WID variation corresponding to the highest current level is below 1% for all measured dies.

In this test chip, each oscillator is implemented using 15 delay elements. Therefore, the variation of the oscillation period is $\sqrt{30} \times \sigma_{t_d}$. Based on these measurements and for the 1 nA bias level, $\sigma_{f_{OSC}} \approx 0.7\%$. Therefore, the variation of the gate delay is expected to be in the range of 3.8%.

A. Experimental Characterization of Jitter

The other undesired effect is the jitter on the edges of the ring oscillator which changes its instantaneous oscillation frequency. Assuming period jitter as the standard deviation σ_τ of

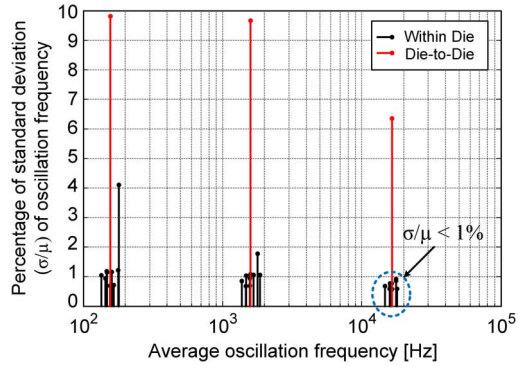

Fig. 11. Standard deviation of oscillation frequency for within-die and die-to die measurements at three different current levels and three different oscillation frequencies.

the oscillation period around its mean value and using an analysis similar to [25], results in:

$$\sigma^2_{\tau,STSCL} = \frac{2kT}{I_{SS} f_{osc} \ln 2}\left(\frac{7}{16U_T} + \frac{1}{V_{SW}}\right) \tag{24}$$

in which f_{osc} is the oscillation frequency, I_{SS} is the tail bias current, V_{SW} is the differential voltage swing at the output of each delay cell and U_T is the thermal voltage. The equation above accounts for the portion of jitter originating from the white noise of the differential pair [M_1 and M_2 in Fig. 1(a)], the tail transistor (M_5) and the load transistors. Similar to [25], jitter is calculated by dividing the total noise voltage by the slope of the differential switching voltage at zero crossing. As opposed to the differential ring oscillator in [25], in the STSCL-based ring oscillator, the differential and tail transistors are biased in subthreshold regime. Therefore, the PSD of the thermal noise at the drain of the transistors is described by [26]:

$$S_{i_n} = 4kTG_{nD} \tag{25}$$

where G_{nD} is defined as:

$$G_{nD} = \frac{n_n}{2} G_m \tag{26}$$

n_n is the subthreshold slope factor of NMOS devices and transconductance in weak inversion is:

$$G_m = \frac{I_D}{n_n U_T} \tag{27}$$

For a CMOS inverter-based and a CMOS differential ring oscillator with differential pair operating in strong inversion, the predicted jitter due to white noise are [25]:

$$\sigma^2_{\tau,inv} = \frac{2kT}{I_{SS} f_{osc}}\left(\frac{1}{V_{DD} - V_{TH}}(\gamma_N + \gamma_P) + \frac{1}{V_{DD}}\right) \tag{28}$$

and

$$\sigma^2_{\tau,diff} = \frac{2kT}{I_{SS} f_{osc} \ln 2}\left(\gamma_N\left(\frac{3}{4V_{effd}} + \frac{1}{V_{efft}}\right) + \frac{1}{V_{SW}}\right) \tag{29}$$

respectively. V_{effd} and V_{efft} stand for the effective gate voltage on the differential pair and tail transistor, and γ_N, γ_p are the thermal noise coefficient of NMOS and PMOS transistors, respectively.

Considering the above equations, while both (28) and (29) are defined by technology-dependant parameters (V_{TH} and γ), (24) only depends on V_{SW}. It is also expected that the variability of the measured jitter in STSCL-based ring oscillators will be less

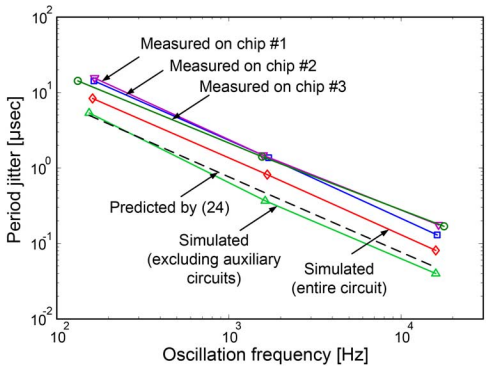

Fig. 12. Measured period jitter versus oscillation frequency for three sample chips. This is compared with prediction based on (24) and simulated jitter, with and without considering auxiliary circuits.

than similar inverter-based and CMOS differential ring oscillators, due to the insensitivity of jitter to the threshold voltage. Improving the matching of the load transistors will reduce the variations of V_{SW} and improve the jitter variability. In addition, in the STSCL topology, the replica bias circuit compensates the effect of temperature and process variations. By comparing the derived equations of jitter, the sensitivity of maximum jitter [i.e., the jitter at minimum V_{SW} based on (24)] to temperature is observed smaller compared to the jitter calculated from (28) and (29), by replacing $V_{SW,min} = 4n_nU_T$ and $U_T = kT/q$ in (24).

The measured period jitter versus oscillation frequency for three sample chips is shown in Fig. 12. The jitter is also simulated[2] in two different conditions, i.e., including and excluding the noise from replica bias, current mirror and current scalers (the tail transistor is included in both cases). The predicted value based on (24) is also plotted against measurement and simulation results. Comparing the two simulation plots, one observation is that flicker noise also affects the jitter of the ring oscillator. This noise mainly originates from the tail and the diode-connected current mirror transistors as well as the input-referred flicker noise of the amplifier in the replica bias circuit. It is worthwhile mentioning that, as shown in [25], the white noise in auxiliary circuits and flicker noise in the differential pair do not contribute to the overall jitter and phase noise. Another reason for the difference between measured and simulated/predicted results is the effect of external noise sources such as substrate and supply noise and the noise on the frequency control current which are not taken into account in simulations and analysis. While at low frequencies, the flicker noise of the tail transistor can cause the simulated jitter to slightly exceed the predicted value only based on white noise, the opposite deviation at higher frequencies is observed. This can be due to the fact that the above analysis is based on the assumption of complete steering of current between the two sides of the differential pair, while in subthreshold region, it is not possible to completely steer the tail bias current to either branch, which can reduce the simulated noise compared to the value predicted by (24).

In this measurement, the oscillation frequency of the ring oscillator is controlled by the bias current with a linear relationship as:

$$f_{osc} \simeq \frac{I_{SS}}{2\ln 2 N_d V_{SW} C_L} \tag{30}$$

[2]Time-domain transient analysis has been used for simulating jitter.

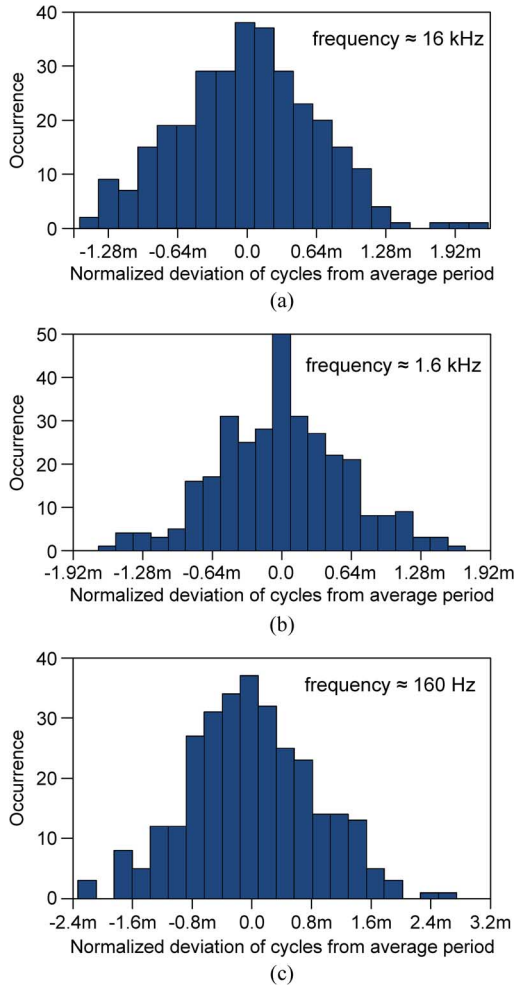

Fig. 13. Simulated histogram of normalized cyclic period deviation from average period $((T-\mu)/\mu)$ for three bias conditions.

where N_d is the number of delay elements in an oscillator ring and C_L is the load capacitance at the output nodes of each delay element. Replacing I_{SS} from (30) in (24) results in:

$$\sigma^2_{\tau,STSCL} \simeq \frac{2kT}{N_d V_{SW} C_L f^2_{osc}} \left(\frac{7}{16U_T} + \frac{1}{V_{SW}}\right) \tag{31}$$

The linear dependency of the period jitter to the oscillation period derived from the above equation is consistent with the measured and simulated results in Fig. 12. The simulated histogram of the cyclic period deviation from the average period for three bias conditions is shown in Fig. 13. This figure demonstrates the dependency of the standard deviation of the period to the bias current and oscillation frequency. Higher frequency (and power consumption) results in smaller value of jitter. For a fixed oscillation frequency, larger values of N_d result in smaller period jitter, which at the same time requires a larger bias current and power consumption. Finally, at a constant frequency and power consumption, increasing the number of delay elements results in smaller tail current and V_{SW} which degrades the overall jitter based on (31).

Another observation is that in the STSCL topology, as opposed to static CMOS inverter-based ring oscillator, the oscillation frequency and jitter are not directly dependant on the supply voltage which guarantees a higher immunity of STSCL-based circuit to supply noise. The sensitivity to supply noise is a major

drawback of inverter-based CMOS ring oscillators, especially at high frequencies [25].

In addition to the speed of operation in the STSCL topology which has low dependency on process variations and can be precisely controlled through bias current, the timing jitter is also independent of the technology-based parameters. Hence, the jitter is more accurately controlled through design parameters such as I_{SS} and V_{SW}. Moreover, as long as the tail bias current (I_{SS}) is much higher than the junction leakage currents and V_{SW} satisfies the necessary condition for the inverter to perform as a logic gate, the oscillator can properly operate even in aggressively scaled deep sub-micron technologies. The proper matching of the load devices and sufficient bandwidth of the amplifier in the replica bias circuit are mandatory to minimize the variations of V_{SW} and provide stable operation of the STSCL-based ring oscillator over a wide range of operation frequencies. This improvement in performance and lower power consumption is achieved at the cost of relatively larger area usage of STSCL-based circuits compared to their CMOS alternatives.

VIII. Conclusions

The effects of process variation on the performance of subthreshold source-coupled logic circuits have been studied and analyzed. This topology is shown very robust against global process, voltage and temperature variations. However, special care is required to overcome the device parameter mismatch effect. Creating an intentional mismatch between on-chip bias generator circuit and the STSCL gates, in addition to the proper device sizing, can help to considerably reduce the circuit sensitivity to parameter mismatches. Experimental results are provided which support the analytical results. Die-to-die and within-die variations are studied and their effects on delay variation of STSCL gates are presented. Jitter measurements of the stand-alone ring oscillators are also presented, and are shown to be consistent with our analytical derivations.

References

[1] C. Piguet, *Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools*. Boca Raton, FL, USA: CRC, 2006.

[2] P. Mroszczyk and P. Dudek, "Tunable CMOS delay gate with improved matching properties," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 9, pp. 2586–2595, 2014.

[3] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 3–29, 2012.

[4] J. Mauricio, F. Moll, and S. Gomez, "Measurements of process variability in 40-nm regular and nonregular layouts," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 365–371, 2014.

[5] T. Sakurai, "Perspectives on power-aware electronics," in *IEEE Int. Solid-State Circ. Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2003, pp. 26–29.

[6] D. Bol, R. Ambroise, D. Flander, and J. D. Legat, "Interests and limitations of technology scaling for subthreshold logic," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 10, pp. 1508–1519, Oct. 2009.

[7] A. Tajalli, E. J. Brauer, Y. Leblebici, and E. Vittoz, "Sub-threshold source-coupled logic circuit design for ultra low power applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1699–1710, Jul. 2008.

[8] B. H. Calhoun, S. Khanna, R. Mann, and J. Wang, "Sub-threshold circuit design with shrinking CMOS devices," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2009, pp. 2541–2544.

[9] M. Pedram and J. Rabaey, *Power Aware Design Methodologies*. Norwell, MA, USA: Kluwer Academic, 2002.

[10] M. Anis and M. Elmasry, *Multi-Threshold CMOS Digital Circuits, Managing Leakage Power*. Norwell, MA, USA: Kluwer Academic, 2003.

[11] H. Soeleman, K. Roy, and B. C. Paul, "Robust subthreshold logic for ultra-low power operation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 9, no. 1, pp. 90–99, Feb. 2001.

[12] A. Tajalli and Y. Leblebici, *Extreme Low Power IC Design: Subthreshold Source-Coupled Mixed-Signal Circuits*. New York: Springer, 2010.

[13] A. Tajalli, M. Alioto, and Y. Leblebici, "Improving power-delay performance of ultra-low-power subthreshold SCL circuits," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 2, pp. 127–131, 2009.

[14] E. Vittoz, "Weak inversion for ultimate low-power logic," in *Low-Power Electronics Design*, C. Piguet, Ed. Boca Raton, FL, USA: CRC, 2005.

[15] J. A. Narud, W. C. Seelbach, and N. Miller, "Relative merits of current mode logic microminiaturization," in *Proc. IEEE Solid-State Circuit Conf. (ISSCC)*, Feb. 1963, pp. 104–105.

[16] J. M. Musicer and J. Rabaey, "MOS current mode logic for low power, low noise CORDIC computation in mixed-signal environment," in *Proc. Int. Symp. Low Power Electron. Design (ISLPED)*, 2000, pp. 102–107.

[17] S. Badel and Y. Leblebici, *Design Automation for Differential MOS Current-Mode Logic Circuits*. New York: Springer, 2011.

[18] M. Alioto and Y. Leblebici, "Analysis and design of ultra-low power subthreshold MCML gates," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2009, pp. 2557–2560.

[19] J. R. Hauser, "Noise margin criteria for digital logic circuits," *IEEE Trans. Educ.*, vol. 36, pp. 363–368, Nov. 1993.

[20] J. Lohstroh, E. Seevinck, and J. De Groot, "Worst-case static noise margin criteria for logic circuits and their mathematical equivalence," *IEEE J. Solid-State Circuits*, vol. 18, pp. 803–807, Dec. 1983.

[21] P. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1212–1224, Jun. 2005.

[22] A. Tajalli and Y. Leblebici, "Subthreshold current-mode delta-sigma quantizer with 3-decade scalable sampling rate and pico-Ampere range resolution," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2010, pp. 174–177.

[23] M. Alioto, G. Palumbo, and M. Pennisi, "Understanding the effect of process variations on the delay of static and domino logic," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 5, pp. 697–710, 2010.

[24] K. Bowman, A. R. Alameldeen, S. T. Srinivasan, and C. B. Wilkerson, "Impact of die-to-die and within-die parameter variations on the clock frequency and throughput of multi-core processors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 12, pp. 1679–1690, Dec. 2009.

[25] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[26] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling*. Hoboken, NJ, USA: Wiley, 2006.

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